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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/029,394	12/28/2001	Jum Soo Kim	054216-5016	2075

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EXAMINER	
NGUYEN, KHIEM D	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 12/23/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/029,394	KIM ET AL.	
	Examiner	Art Unit	
	Khiem D Nguyen	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 October 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 December 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Amendment

Response to Arguments

Applicant's arguments with respect to claims 1-12 have been considered but are moot in view of the new ground(s) of rejection.

New Grounds of Rejection

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the features as recited in present claim 7, lines 11-15 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in-
(1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
(2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

Claims 1-12 are rejected under 35 U.S.C. 102(e) as being anticipated by Fang (U.S. Patent 6,316,293).

In re claim 1, **Fang** discloses a method of manufacturing a code address memory cell, the method comprising the steps of: forming a gate insulating film **(FIGS. 7a-b: ONO)** in which a plurality of oxide films and nitride films (col. 7, lines 4-25) are stacked on a surface of a semiconductor substrate **(FIGS. 7a-b: P-WELL)**; forming a polysilicon film **(FIGS. 7a-b: Poly2)** on the gate insulating film; etching given regions of the polysilicon film and the gate insulating film to form a gate **(FIGS. 7a-b)**; and performing an impurity ion implantation process to form a source region **(FIGS. 7a-b: S)** and a drain region **(FIGS. 7a-b: D)** (col. 8, lines 29-65 and FIGS. 6a-7b).

In re claims 2 and 4, **Fang** discloses wherein the gate insulating film **(FIGS. 7a-b: ONO)** is formed by stacking at least two or more layers of at least one of the oxide and nitride film.

In re claim 3, **Fang** discloses wherein the gate insulating film has a thickness of 285 Angstroms (col. 7, lines 4-25).

In re claims 5 and 6, **Fang** discloses wherein the gate insulating film is formed by stacking a first oxide film, a first nitride film, a second oxide film, a second nitride film and a third oxide film **(FIGS. 7a-b)**.

In re claim 7, **Fang** discloses a method of manufacturing a code address memory cell in a peripheral circuit region and a flash memory cell in a cell region, the method comprising the steps of: forming a device isolation film in a give region on a semiconductor substrate to define an active region and a device isolation region **(FIGS.**

6a-7b); defining the active region into a cell region **(FIG. 7a)** and a peripheral circuit region **(FIG. 7b)** by a given process; forming a tunnel oxide film **(FIG. 7a: Tunnel oxide)** and a first polysilicon film **(FIG. 7a: Poly1)** on the entire circuit and then patterning the tunnel oxide film and the first polysilicon film so that the tunnel oxide film and the first polysilicon film can only remain in a give region of the cell region, thus defining a floating gate; forming an insulating film **(FIG. 7a: ONO)** in which an oxide film and a nitride film (col. 7, lines 4-25) are stacked on the entire structure to form a second polysilicon film **(FIG. 7a: Poly2)**; patterning the second polysilicon film and the insulating film so that they can remain only in a given region of the cell region and the peripheral circuit region, thus forming a control gate in the cell region **(FIG. 7a)** and a gate **(FIG. 7b: Poly2)** in the peripheral circuit region; and performing an impurity ion implantation process for a give region of the semiconductor substrate to form a source region **(FIG. 7a: S)** and a drain region **(FIG. 7b: D)**, so that a flash memory cell is formed in the cell region, and a code address memory cell is formed in the peripheral circuit region (col. 8, lines 29-65 and FIGS. 6a-7b).

In re claims 8 and 10, **Fang** discloses wherein the gate insulating film **(FIGS: 7a-b: ONO)** is formed by stacking at least two or more layers of at least one of the oxide and nitride film (col. 7, lines 4-25).

In re claim 9, **Fang** discloses wherein the gate insulating film has a thickness of 285 Angstroms (col. 7, lines 4-25).

In re claims 11 and 12, **Fang** discloses wherein the gate insulating film is formed by stacking a first oxide film, a first nitride film, a second oxide film, a second nitride film and a third oxide film **(FIGS. 7a-b)**.

Response to Amendment

Response to Arguments

Applicant's arguments with respect to claims 1-12 have been considered but are moot in view of the new ground(s) of rejection.

Objection to the Drawings is maintained because every features of the invention specified in the claims are not shown in FIG. 4 since FIG. 2 was described in the Specification as a Prior Art.

In response to Applicant's argument that Shirai does not teach or suggest at least the step of "forming a gate insulating film in which a plurality of oxide films and nitride films are stacked on a surface of a semiconductor substrate" as recited by amended independent claim 1 and "patterning the second polysilicon film and the insulating film so that they can remain only in a give region of the cell region and the peripheral circuit region, thus forming a control gate on the floating gate in the cell region, and a gate on a surface of the substrate in the peripheral circuit region" as recited by amended independent claim 7, examiner respectfully disagree, Applicants are directed to the new ground(s) of rejection presented in this Office Action where the newly discovered reference Fang (U.S. Patent 6,316,293) discloses the discussed features.

For these reasons, examiner holds the rejection proper.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a). A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khiem D Nguyen whose telephone number is (703) 306-0210. The examiner can normally be reached on Monday-Friday (8:00 AM - 5:00 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (703) 306-2794. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305-3432 for regular communications and (703) 305-3432 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

K.N.
December 18, 2003

W. David Coleman
Primary Examiner